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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,169	03/01/2004	Adrian C. Moga	BEA920030024US1	1020

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

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08/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,169	MOGA ET AL.	
	Examiner	Art Unit	
	ZHUO H. LI	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/17/2008 has been entered.

Response to Amendment

2. This Office action is in response to the amendment filed on 7/17/2008, claims 1-17 are pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 9-11, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Irie et al. (US PAT. 6,038,644 hereinafter Irie).

Regarding claim 1, Irie discloses a cache-coherent system, i.e., multiple processing system (figure 1), comprising a memory having a plurality of memory units (col. 3 line 66

through col. 4 line 4), a plurality of nodes, i.e., processing units (10-1 to 10-n) employing a coherence protocol to maintain cache coherence of the memory (col. 4 lines 5-29), a cache (300, figure 1) within each node to temporarily store contents of the plurality of memory units (col. 4 lines 10-16), and logic, i.e., multicast table control unit (450, figure 1) within each of node (figure 1) to determine whether a cache miss, i.e., snooping operation perform when requested is missing in the requested processing unit (col. 4 lines 30-32, and col. 5 line 27 through col. 6 line 14), relating to a memory unit should be transmitted only to a sub-plurality of nodes lesser in number than the plurality of nodes but greater than one, based on a criteria, i.e., the multicast table control unit (450) uses the destination information stored within multicast table (400, figure 1) to generate coherence requested to only part of the processor units which are likely to have a copy of the data and to one of the memory units, which does not transfer to all other processor units based on the destination information related to the coherent processing request (col. 4 lines 30-45, col. 7 line 44 through col. 8 line 21, and col. 9 line 1 through col. 12 line 67).

Regarding claim 2, Irie discloses a cache-coherent system wherein the criteria includes whether, to ultimately reach an owning node for the memory unit (col. 9 line 1 through col. 12 line 67), such transmission is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency as compared to broadcasting the cache miss to all of the plurality of nodes (col. 4 lines 46-58).

Regarding claim 9, Irie discloses a method comprising determining at a first node, i.e., processing unit (10-i) whether a cache miss relating to a memory unit of a shared memory system, i.e., multiple processing system (figure 1) of a plurality of nodes, i.e., processing units (10-1 to 10n, figure 1) including the first node and employing a coherence protocol should be

selectively broadcast only to a sub-plurality of nodes lesser in number than the plurality of nodes but greater than one based on a criteria, i.e., only transfer to part of the processing units which are likely to have a copy of the data by the determination of the destination information stored within the multicast table (400, figure 1) and (col. 4 lines 30-45, col. 5 lines 28 through col. 6 line 14), and in response to determining that the cache miss should be selectively broadcast only to the sub-plurality of nodes, i.e., destination information stored within the multicast table (col. 4 lines 35-45, col. 9 line 1 through col. 12 line 33), selectively broadcasting the cache miss by the first node only the sub-plurality of nodes (col. 11 line 46 through col. 12 line 67).

Regarding claim 10, Irie discloses a method further comprising in response to determining that the cache miss should not be selectively broadcast to the sub-plurality of nodes, broadcasting the cache miss by the first node to all of the plurality of nodes (col. 8 lines 49-67).

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth in claims 9 and 11.

Regarding claims 16-17, the limitations of the claims are rejected as the same reasons set forth in claims 1 and 2.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 3-8, and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irie et al. (US PAT. 6,038,644 hereinafter Irie) in view of Steely, JR. et al. (US 2005/0160430 hereinafter Steely).

Regarding claim 3, Irie differs from the claimed invention in not specifically teaches the cache-coherent system wherein the logic within each node is to determine whether the node is a home node for the memory unit to which the cache miss relates in determining that transmission to the sub-plurality of node lesser in number than the plurality of nodes is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency to ultimately reach the owning node for the memory unit. However, Steely teaches a multi-processor system including an owner predictor control, i.e., logic, that a processor is operable to generate two parallel requests for a desired cache line in response to cache miss, i.e., one request to home node and another request to predicted target processors as predicted by the owner predictor control, in order to reduce latency associated with retrieving data ([0054] through [0056]). Therefore, it

would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the coherent system of Irie in having logic within each node is to determine whether the node is a home node for the memory unit to which the cache miss relates in determining that transmission to the sub-plurality of node lesser in number than the plurality of nodes is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency to ultimately reach the owning node for the memory unit, as per teaching by Steely, because it reduces latency associated with retrieving data.

Regarding claim 4, Steely discloses the system wherein the sub-plurality of nodes comprises an owning node (i.e. predicted target processors) for the memory unit as stored at a directory of the home node ([0050]).

Regarding claim 5, Steely discloses the system wherein the logic, i.e., owner predictor control, within each node to determine whether the cache of the node has stored a hint, as to a potential owning node for the memory unit as a result of an earlier event in determining that transmission to the sub-plurality of nodes lesser in number than the plurality of nodes is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency to ultimately reach the owning node for the memory unit (([0050] and [0054] through [0056]).

Regarding claim 6, Irie discloses the system wherein the event includes an invalidation of the memory unit by the potential owning node (col. 6 lines 4-14, col. 9 line 36 through col. 11 line 5).

Regarding claim 7, Steely discloses the system wherein the sub-plurality of nodes comprises a home node (180, figure 3) of the memory, and the potential owning node (i.e. predicted target processors) for the memory unit ([0055] through [0056]).

Regarding claim 8, Steely discloses the system wherein the logic, i.e., owner predictor control, within each node is to determine whether the memory unit relates to a predetermined memory sharing pattern encompassing the one or more nodes in determining that transmission to the one of more nodes lesser in number than the plurality of nodes is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency to ultimately reach the owning node for the memory unit ([0017]).

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 13, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Response to Arguments

7. Applicant's arguments with respect to claim1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Glasco (US PAT. 7,107,409) discloses methods and apparatus for speculative probing at a request cluster in a multiple processing system.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ZHUO H. LI whose telephone number is (571)272-4183. The examiner can normally be reached on Mon - Fri 6:00am - 2:30pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zhuo H Li/
Examiner, Art Unit 2185

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185